Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended) A microelectronic device comprising:

a die fixed within an opening in a package core by an encapsulation material between said die and said package core; and

a single metallization layer built up upon said die and said package core, said single metallization layer being directly connected to conductive contacts on an upper surface of said die and having a plurality of landing pads that are spaced for direct connection to an external circuit board.

2. (original) The microelectronic device of claim 1, wherein:

said plurality of landing pads includes a first group of landing pads situated above said die and a second group of landing pads situated above said package core.

3. (original) The microelectronic device of claim 1, wherein:

said die includes a plurality of bond pads on a surface thereof, wherein said plurality of landing pads on said single metallization layer has a pitch that is significantly greater than a pitch of said plurality of bond pads.

4. (original) The microelectronic device of claim 3, wherein:

said pitch of said plurality of landing pads is at least two times greater than said pitch of said plurality of bond pads.

5. (original) The microelectronic device of claim 1, wherein:

said die includes a plurality of power bars and a plurality of ground bars within a central portion of an upper surface thereof, wherein said single metallization layer includes at least one landing pad that is conductively coupled to multiple power bars within said plurality of power bars through corresponding via connections.

6. (original) The microelectronic device of claim 5, wherein:

said single metallization layer includes at least one landing pad that is conductively coupled to multiple ground bars within said plurality of ground bars through corresponding via connections.

7. (original) The microelectronic device of claim 1, wherein:

said die includes a plurality of signal bond pads distributed within a peripheral region of a surface thereof.

8. (original) The microelectronic device of claim 7, wherein:

said plurality of landing pads within said single metallization layer includes a first signal landing pad that is situated above said package core, said first landing pad being conductively coupled to a first signal bond pad of said die.

9. (original) The microelectronic device of claim 8, wherein:

said single metallization layer includes a first transmission line segment to facilitate signal communication between said first signal landing pad and said first signal bond pad.

10. (original) The microelectronic device of claim 9, wherein:

said first transmission line segment includes a microstrip transmission structure.

11. (original) The microelectronic device of claim 9, wherein:

said package core includes a metallic cladding on an upper surface thereof, said metallic cladding providing a ground structure for said first transmission line segment.

12. (original) The microelectronic device of claim 11, wherein:

said plurality of landing pads within said single metallization layer includes a ground pad situated above said package core, said ground pad being conductively coupled to said metallic cladding on said package core through at least one via connection.

13. (original) The microelectronic device of claim 1, wherein:

said die includes signal bond pads along two opposing edges of an upper surface thereof, wherein said single metallization layer includes a plurality of conductive lines that are conductively coupled to said signal bond pads on said two opposing edges of said upper surface of said die.

14. (original) The microelectronic device of claim 13, wherein:

said single metallization layer includes a power plane occupying portions of said single metallization layer unoccupied by said plurality of conductive lines.

15. (original) The microelectronic device of claim 1, wherein:

said single metallization layer includes a plurality of power strips and a plurality of ground strips in a region above said die, said power strips being conductively coupled to power bond pads on said die through corresponding via connections and said ground strips being conductively coupled to ground bond pads on said die through corresponding via connections.

16. (original) The microelectronic device of claim 15, wherein:

said package core includes a conductive cladding on a surface thereof; and

said single metallization layer includes at least one ground strip that extends out over said package core, said at least one ground strip being conductively coupled to said conductive cladding of said package core through at least one via connection.

17. (original) The microelectronic device of claim 15, comprising:

at least one decoupling capacitor connected between a first power strip and a first ground strip on said single metallization layer.

18. (original) The microelectronic device of claim 1, wherein:

said package core includes a conductive cladding on at least one surface thereof.

19. (original) The microelectronic device of claim 1, wherein:

said microelectronic device is a microprocessor.

20. (currently amended) An electrical system comprising:

a microelectronic device having:

a die fixed within a package core by an encapsulation material; and

a single metallization layer built up upon said die and said package core, said single metallization layer being directly connected to conductive contacts on an upper surface of said die and having a plurality of landing pads; and

a circuit board having a conductive pattern on a first side thereof, said conductive pattern including a plurality of conductive elements;

wherein said microelectronic device is mounted on said circuit board so that said plurality of landing pads on said single metallization layer of said microelectronic device are aligned with and connected to said plurality of conductive elements within said conductive pattern of said circuit board.

21. (original) The electrical system of claim 20, comprising:

at least one capacitor mounted on a second side of said circuit board to provide decoupling for circuitry within said die.

22. (original) The electrical system of claim 20, wherein:

said circuit board includes a computer motherboard.

23. (original) The electrical system of claim 20, wherein:

said microelectronic device includes a microprocessor.

24. (original) The electrical system of claim 20, wherein:

said microelectronic device is mounted on said circuit board using one of the following techniques: ball grid array, land grid array, pin grid array, and surface mount technology.

25. (original) The electrical system of claim 20, wherein:

said plurality of landing pads includes at least one power landing pad overlapping said die that is conductively coupled to a plurality of power bond pads on said die.

26. (original) The electrical system of claim 25, wherein:

said plurality of landing pads includes at least one ground landing pad overlapping said die that is conductively coupled to a plurality of ground bond pads on said die.

27. (original) The electrical system of claim 20, wherein:

said plurality of landing pads includes at least one signal landing pad overlapping said package core that is conductively coupled to a signal bond pad on said die through a transmission line segment and at least one via connection.

28. (original) The electrical system of claim 27, wherein:

said package core includes a metallic cladding on a surface thereof, said metallic cladding forming a ground plane for said transmission line segment.

29. (original) A microelectronic device comprising:

a package core having an opening therein;

a die fixed within said opening of said package core by an encapsulation material, said die having a plurality of conductive contacts on an upper surface thereof;

a dielectric layer disposed over an upper surface of said package core and said upper surface of said die; and

a single metallization layer disposed upon said dielectric layer, said single metallization layer being conductively coupled to said plurality of conductive contacts on said upper surface of sad die through a plurality of via connections, said single metallization layer having a plurality of landing pads that are spaced for direct connection to an external circuit board, said plurality of landing pads including at least one landing pad above said die and at least one landing pad above said package core.

30. (original) The microelectronic device of claim 29, wherein:

said package core includes a copper cladding on an upper surface thereof that forms a ground plane for a transmission structure within said single metallization layer.

31. (currently amended) The microelectronic device of claim ~~29~~ 30, wherein:

said plurality of landing pads includes at least one ground pad that is conductively coupled to said copper cladding of said package core through one or more via connections.

32. (original) The microelectronic device of claim 29, wherein:

said die includes a plurality of power bars and ground bars within a central region of said upper surface and a plurality of signal pads within a peripheral region of said upper surface.

33. (original) The microelectronic device of claim 32, wherein:

said single metallization layer includes at least one power landing pad disposed above said die, said at least one power landing pad being conductively coupled to multiple power bars on said die through corresponding via connections.

34. (original) The microelectronic device of claim 33, wherein:

said single metallization layer includes at least one ground landing pad disposed above said die, said at least one ground landing pad being conductively coupled to multiple ground bars on said die through corresponding via connections.

35. (original) The microelectronic device of claim 34, further comprising:

at least one capacitor coupled between said at least one ground landing pad and said at least one power landing pad.

36. (original) The microelectronic device of claim 29, wherein:

said single metallization layer includes at least one signal landing pad disposed above said package core, said at least one signal landing pad being conductively coupled to a signal bond pad on said die.

37. (original) The microelectronic device of claim 29, comprising:

at least one decoupling capacitor fixed within said opening of said package core by said encapsulation material, said single metallization layer including conductive traces to connect contacts of said at least one decoupling capacitor to power and ground contacts on said upper surface of said die.

38. (new) The microelectronic device of claim 29, wherein:

a bottom surface of said dielectric layer is above said upper surface of said die and said upper surface of said package core.

39. (new) The microelectronic device of claim 29, wherein:

an upper surface of said dielectric layer is below a top surface of said single metallization layer.

40. (new) The microelectronic device of claim 1, wherein:

said opening extends from a top surface of said package core to a bottom surface of said package core.

41. (new) The microelectronic device of claim 1, wherein:

said package core includes a floor beneath said opening.

42. (new) The microelectronic device of claim 1, wherein:

said upper surface of said die, an upper surface of said encapsulation material and an upper surface of said package core are substantially flush.

43. (new) The microelectronic device of claim 1, further comprising:

a dielectric layer disposed on said die, said encapsulation material, and said package core.

44. (new) The microelectronic device of claim 1, further comprising a conductive cladding layer disposed directly on the package core and covering substantially all of the area of a top surface of the package core.

45. (new) The microelectronic device of claim 2, wherein the plurality of landing pads of the single metallization layer include a plurality of signal landing pads and wherein all of the signal landing pads are situated above the package core and none of the signal landing pads are situated above the die.

46. (new) A microelectronic device comprising:

a package core;

a die fixed within said package core by an encapsulation material between said die and said package core; and

a single metallization layer built up upon said die and said package core, said single metallization layer having a plurality of landing pads that are spaced for direct connection to an external circuit board, wherein an upper surface of said die, an upper surface of said encapsulation material and an upper surface of said package core are substantially flush.

47. (new) The microelectronic device of claim 46, further comprising:

a dielectric layer disposed on said package core, said die, and said encapsulation material, wherein said dielectric layer comprises a top surface, and said top surface is substantially below a top surface of said single metallization layer.

48. (new) The microelectronic device of claim 46, further comprising:

a conductive cladding disposed on said package core.

49. (new) The microelectronic device of claim 48, wherein:

said die includes a plurality of conductive contacts; and

said single metallization layer includes a plurality of signal landing pads and at least one ground pad, wherein at least one of said signal bond pads is conductively coupled to at least one of said conductive contacts by a transmission line segment, and said ground pad is conductively coupled to said conductive cladding.